SEL is high. Channel status information is displayed for the channel selected by CS12. C0, which is channel status bit 0, defines professional ($\overline{C0}=0$)or consumer ($\overline{C0}=1$) mode and further controls the definition of the Ca-Ce pins. These pins are updated with the rising edge of CBL.

CS12 Channel Select, pin 13
This pin is also dual function and is selected by bringing SEL high. CS12 selects sub-frame 1 (when low) or sub-frame 2 (when high) to be displayed by channel status pins $\overline{C0}$ and Ca through Ce

FCK Frequency Clock, pin 13
Frequency clock input that is enabled by bringing SEL low. FCK is compared to the received clock frequency with the value displayed on F2 through F0. Nominal input value is 6.144 MHz.

E0, E1, E2 Error Condition, pins 4-6
Encoded error information that is enabled by bringing SEL low. The error codes are prioritized and latched so that the error code displayed is the highest level of error since the last clearing of the error pins. Clearing is accomplished by bringing SEL high for more than 8 MCK cycles.

F0, F1, F2 Frequency Reporting Bits, pins 2-3, 27
Encoded sample frequency information that is enabled by bringing SEL low. A proper clock on FCK must be input for at least two thirds of a channel status block for these pins to be valid. They are updated three times per block, starting at the block boundary. These pins are invalid when the PLL is out of lock.

ERF Error Flag, pin 25
Signals that an error has occurred while receiving the audio sample currently being read from the serial port. Three errors cause ERF to go high: a parity or biphase coding violation during the current sample, or an out of lock PLL receiver.

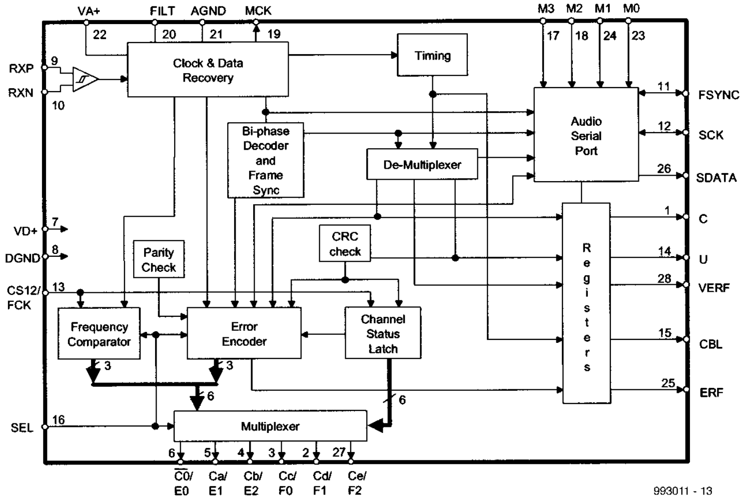
Receiver interface

RXP, RXN Differential Line Receivers, pins 9, 10
RS422 compatible line receivers.

Phase Locked Loop

MCK Master Clock, pin 19
Low jitter clock output of 256 times the received sample frequency.

FILT Filter, pin 20
An external 470Ω resistor and 0.068µF capacitor is required from FILT input to analog ground.



CS8414 Block Diagram.

CS8414
96 kHz Digital Audio Receiver

Manufacturer

CRYSTAL®
A DIVISION OF CIRRUS LOGIC

Cirrus Logic, Inc., Crystal Semiconductor Division,
P.O. Box 17847, Austin, Texas 78760, U.S.A.
Tel. (512) 445 7222, fax (512) 445 7581.
Internet: http://www.crystal.com

Features

- Sample rates to > 100 kHz
- Low-Jitter, On-Chip Clock recovery
- 256xFs Output clock Provided
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ
- CP340/1201 Professional and Consumer Formats
- Extensive Error Reporting
- Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Pin Compatible with CS8411 and CS8412

Ordering information
CS8414-CS 0º to 70º C 28-pin plastic SOIC

Application example
Audio DAC 2000,
Elektor Electronics November 1999.

Description
The CS8414 is a monolithic CMOS device which receives and decodes audio data up to 96 kHz according to the AES/EBU, IEC958, S/PDIF and EIAJ CP340/1201 interface standards. The CS8414 receives data from a transmission line, recovers the clock and synchronization signals, and demultiplexes the audio and digital data. Differential and single-ended inputs can be decoded.

Normal Audio Port modes (M3 = 0)			
M2	**M1**	**M0**	**Format**
0	0	0	0 – Out, L/R, 16-24 Bits
0	0	1	1 – In, L/R, 16-24 Bits
0	1	0	2 – Out, L/R, I^{2}S Compatible
0	1	1	3 – In, L/R, I^{2}S Compatible
1	0	0	4 – Out, WSYNC, 16-24 bits
1	0	1	5 – Out, L/R, 16 Bits LSBJ
1	1	0	6 – Out, L/R, 18 Bits LSBJ
1	1	1	7 – Out, L/R, MSB Last

The CS8414 de-multiplexes the channel, user and validity data directly to serial output pins with dedicated output pins for the most important channel status bits. The CS8414 does not need a microprocessor to handle the non-audio data (although a micro may be used with the C and U ports). Instead, dedicated pins are available for the most important channel status bits. The CS8414 is a monolithic CMOS circuit that receives and decodes digital audio data which was encoded according to the digital audio interface standards. It contains an RS422 line receiver and clock and data recovery utilizing an on-chip phase-locked loop. The audio data is output through a configurable serial port that supports 14 formats. The channel status and user data have their own serial pins and the

Special Audio port Modes (M3=1)			
M2	**M1**	**M0**	**Format**
0	0	0	8 – Format 0 – No repeat on error
0	0	1	9 – Format 1 – No repeat on error
0	1	0	10 – Format 2 – No repeat on error
0	1	1	11 – Format 0 – Async. SCK input
1	0	0	12 – Received NRZ Data
1	0	1	13 – Received Bi-phase Data
1	1	0	14 - Reserved
1	1	1	15 – CS8414 Reset

validity flag is OR'ed with the ERF flag to provide a single pin, VERF, indicating that the audio data may not be valid. This pin may be used by interpolation filters that provide error correction.

Pin descriptions

Power Supply Connections

VD+ Positive Digital Power, pin 7
Positive supply for the digital section. Nominally +5 volts.

VA+ Positive Analog Power, pin 22
Positive supply for the analog section. Nominally +5 volts.

DGND Digital Ground, pin 18
Ground for the digital section. DGND should be connected to the same ground as AGND.

AGND Analog Ground, pin 21
Ground for the analog section. AGND should be connected to the same ground as DGND.

Audio Output Interface

SCK Serial Clock, pin 12
Serial clock for SDATA pin which can be configured (via the M0, M1, M2 and M3 pins) as an input or output, and can sample data on the rising and falling edge. As an output, SCK will generate 32 clocks for every audio sample. As an input, 32 SCK periods per audio sample must be provided in all normal modes.

FSYNC Frame Sync, pin 11
Delineates the serial data and may indicate the particular channel, left or right, and may be an input or output. The format is based on M0, M1, M2 and M3 pins.

SDATA Serial Data, pin 26
Audio data serial input pin

M0, M1, M2, M3 Serial Port Mode Select, pins 23, 24, 18, 17
Selects the format of FSYNC and the sample edge of SCK with respect to SDATA. M3 selects between eight normal modes (M3=0), and six special modes (M3=1).

Control Pins

VERF Validity + Error Flag, pin 28
A logical OR'ing of the validity bit from the received data and the error flag. May be used by interpolation filters to interpolate through errors.

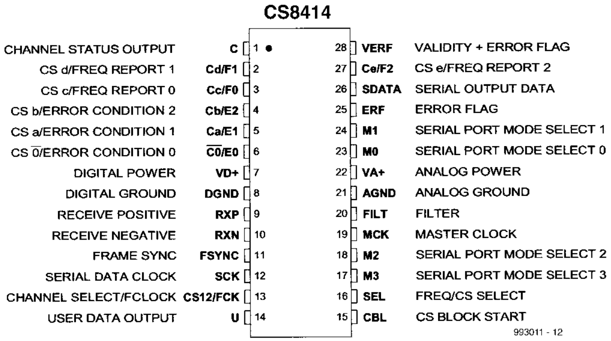
U User bit, pin 14
Received user bit serial output port. FSYNC may be used to latch this bit externally. (Except in I^{2}S modes when this pin is updated on the active edge of FSYNC).

C Channel Status Output, pin 1
Received channel status bit serial output port. FSYNC may be used to latch this bit externally. (Except in I^{2}S modes when this pin is updated on the active edge of FSYNC).

CBL Channel Status Block Start, pin 15
The channel status block output is high for the first four bytes of channel status and low for the last 20 bytes.

SEL Select, pin 16
Control pin that selects either channel status information (SEL = 1) or error and frequency information (SEL = 0) to be displayed on six of the following pins.

$\overline{\text{C0}}$, Ca, Cb, Cc, Cd, Ce Channel Status Output Bits, pins 2-6, 27
These pins are dual function with the 'C' bits selected when



CS8414 Pinout.

Absolute maximum ratings (GND = 0V, all voltages with respect to ground)

Parameters	Symbol	Min.	Max.	Unit
Power Supply Voltage	VD+, VA+	-	6.0	V
Input Current, Any Pin Except Supply (Note 1)	I_{in}	-	±10	mA
Input Voltage, Any Pin Except RXP, RXN	V_{IN}	–0.3	(VD+) + 0.3	mA
Input Voltage, RXP and RXN	V_{IN}	–12	12	V
Storage Temperature	T_{stg}	–65	150	ºC

Notes: 1. Transient currents of up to 100 mA will not cause SCR latch-up

Recommended operating conditions (GND = 0V, all voltages with respect to ground)

Parameters	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	VD+, VA+	4.75	5.0	5.25	V
Supply Current VA+	I_A	-	20	30	mA
Supply Current VD+	I_D	-	20	30	mA
Ambient Operating Temperature: (note 2)	T_A	0	25	70	ºC
Power Consumption	P_D	-	175	315	mW

Notes: 2. The -CS parts are specified to operate over 0 to 70ºC but are tested at 25ºC only.

Digital characteristics (TA = 25ºC; VD+, VA+ = 5V ±5%)

Parameters	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage, except RXP, RXN	V_{IH}	2.0	-	-	V
Low-Level Input Voltage, except RXP, RXN	V_{IL}	-	-	+0.4	V
High-Level Output Voltage (I_O = 200µA)	V_{OH}	(VD+) – 1.0	-	-	V
Low-level Output Voltage (I_O = –3.2mA)	V_{OL}	-	-	0.5	V
Input Leakage Current	I_{in}	0	1.0	10	µA
Input Sample frequency (Note 3)	F_S	28.4	-	100	kHz
Master Clock Frequency (Note 3)	MCK	7.28	256xF_S	25.6	MHz
MCK Clock Jitter	t_j	-	200		psRMS
MCK Duty Cycle (high time/cycle time)		-	50	-	%

Notes: 3. F_S is defined as the incoming audio sample frequency per channel.